Fermi National Accelerator Laboratory

PIXEL DETECTOR PROJECT

FPIX0 READOUT CONTROLLER

Document # ESE-PIX-19981001

-PRELIMINARY-

March 12, 1999

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1 GENERAL INFORMATION

This document describes the 1st Fermilab Pixel chip (FPIX0), the Pixel Readout Controller Board (FPRB0), and the Pixel Detector Test Stand. The objective of the Test Stand is to exercise Pixel Detectors under a beam test condition at Fermilab. The beam test will try to determine the spatial resolution of the Pixel Detector including the use of charge sharing as measured by an analog read out. The detector will be oriented at various angles to the beam and read out the pulse height on each pixel to study how the resolution varies as a function of many parameters. To measure the resolution a high precision telescope will be installed based on an existing set of silicon strip planes. It will be able to measure the residual distribution between the telescope's prediction and the pixel detector measurement. To study these effects with 4 to 10 μm of resolution, high momentum tracks are needed to minimize the effect of multiple scattering. Because of the small size of the pixel chip (3.2 mm by 4.4 mm of active area), a beam of 100 GeV with an intensity of about 10-100KHz/cm^2 is needed.

Therefore, this test stand must be capable to control and readout two different types of detectors: Silicon Strip and Pixels.

The Test Stand will operate in a test beam with the following characteristics:

a) In a 90 sec. period, the spill beam will be available for 45 sec. The next 45 sec. will not have any beam.
b) Of this 45 sec., bunches will be available, in AVERAGE, each 10 μs. There is no information regarding when bunches will be actually available during this 45 sec.

The Accelerator Division will provide a 53 MHz clock and a Start of Spill signal. The Start of Spill will signal when the spill is about to start, and it will occur one second or earlier before the 45 sec. spill starts.

A VME based test stand was developed to test Silicon Detectors [1] and SVX-II chips [2]. This test stand controls the four operation modes of the SVX-II chips: acquisition, digitization, readout and configuration. The data read out from the SVX-II chips are stored inside data buffers for later transfer to a SGI workstation. The Pixel Detector Test Stand will use the same units developed for the Silicon Detector Test Stand, in addition to a specific module to control and readout the Pixel Detector itself.

Figure 1 shows the main components of the Pixel Detector Test Stand:

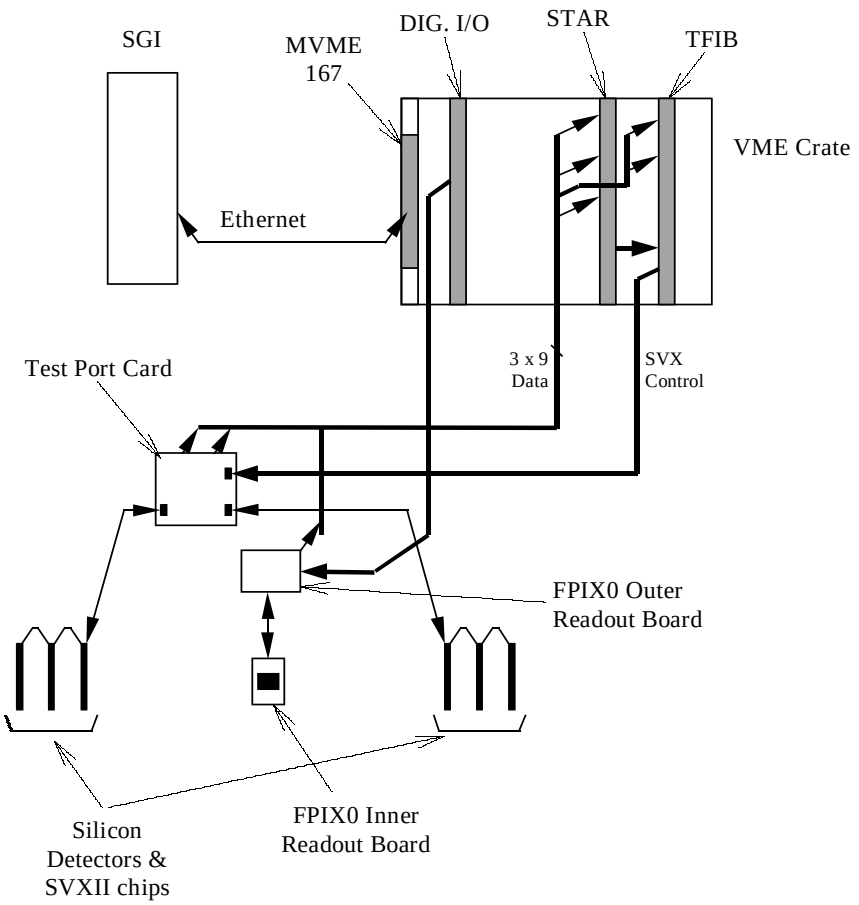

Figure 1 Test Stand Configuration

a) A SGI microcomputer that controls the VME crate through a Motorola MVME167 [3].
b) The Silicon Test Asynchronous Readout (STAR) VME module [4].
c) Test Fiber Interface Board (TFIB) [5].
d) Test Port Card (TPC) [6].
e) Fermilab Pixel Readout Board (FPRB0), which comprehends two modules: the Inner and Outer Readout Boards.
f) Digital VME I/O interface [7].

In this document we will specify the FPRB0 module. For the specification of the other modules or operation of the test stand for the Silicon Detector, please, refer to the appropriate documentation.

The main functions of the FPRB0 are as follows:
a) read out of the digital and analog data stored in the Pixel Chip,
b) test the Pixel Chip by injecting charge in the pre-amplifiers and then reading it out,
c) accept external triggers from the Scintilators and the VME
d) supply bias currents and voltages to the Pixel Chip.

The FPRB0 board executes the readout of the FPIX0 chip (for more details regarding FPIX0 refer to Appendix C), and it is also responsible for passing the signals from the RS485 to the FPIX0 in the initialization cycle. Figure 2 shows the block diagram of the FPRB0. The FPRB0 and the FPIX0 chip is controlled by the Control Logic, which is programmed in firmware in a EPLD part of Altera. Other units

comprehend several interfaces and voltage regulators. The RS485 interface connects to the VME Digital I/O board, and the PECL Start Interface transmits the data to the STAR.

The readout is externally triggered by a NIM, ECL or RS485 (VME) trigger signal. During readout the FPRB0 adds a header, a trailer and Scintilator Coincidence Count Information and transmits the information to the STAR. The pixel data is zero suppressed, only hit pixels are read out. This data include the Pixel location in the array plus a 7 bit digitized value of the peak analog voltage generated by the front-end amplifier. We will now discuss in details the functions of the FPRB0.

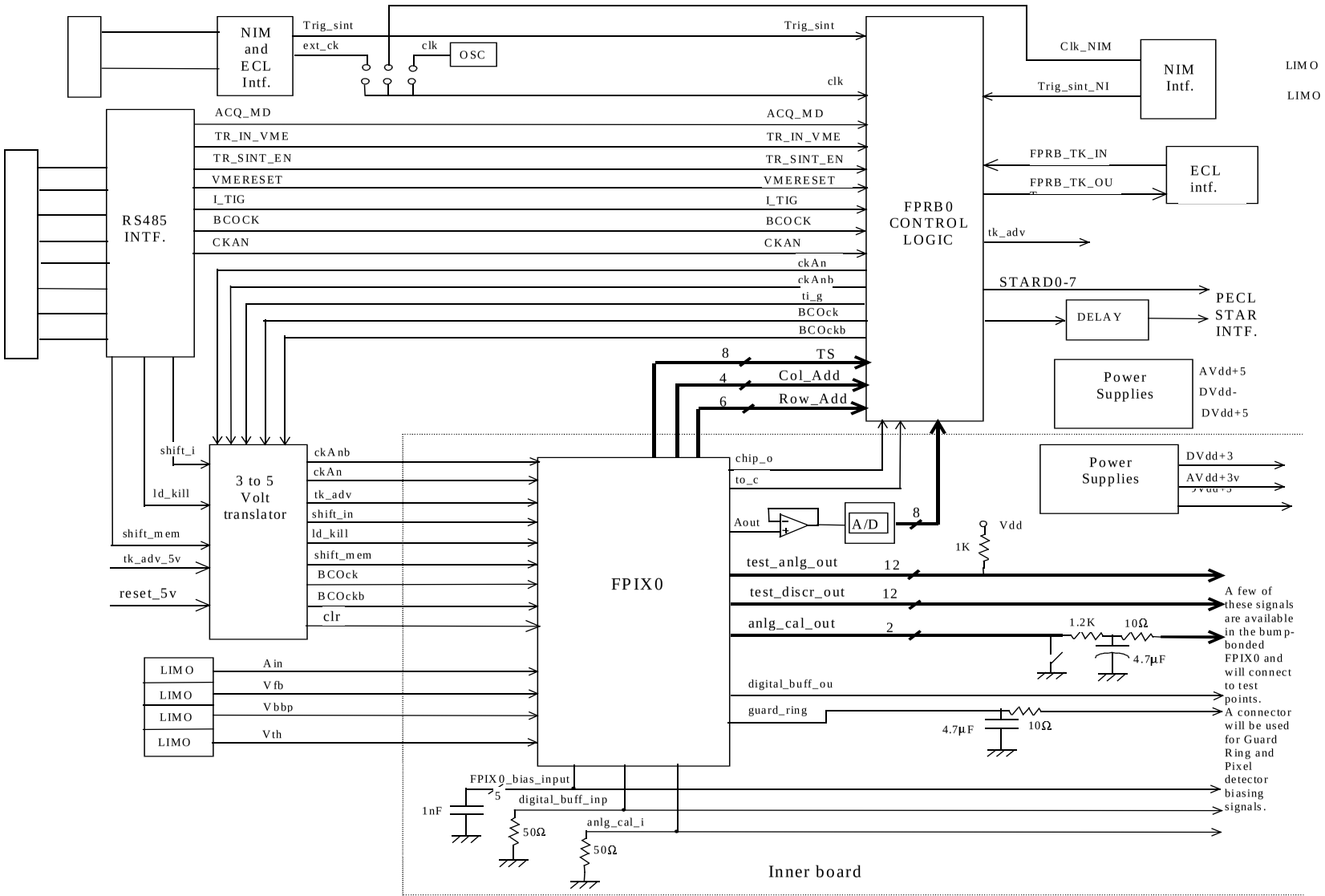

Figure 2. FPRB0 block diagram

2 FPRB0 OPERATION MODES

2.1 Initialization

The initialization of the FPIX0 requires loading the 768 bit kill and injection shift registers (see Figure 3). This register runs from the bottom of the rightmost column (i.e column 11, row 0), to the top of column 11. The register has a serpentine pattern: the top of column 11 (the rightmost) is chained with the top of column 10, runs to the bottom of column 10 and is chained with the bottom of column 9 and so on. To enable the kill and charge injection an logic one must be stored in that specific pixel cell.

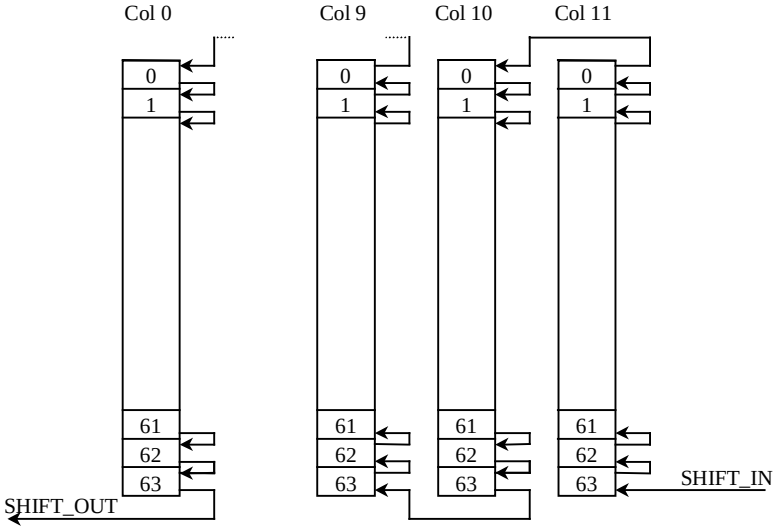

Figure 3. Kill/Charge in

Figure 4 shows the initialization sequence. For the configuration of the FPIX0:

- The RS485 inputs ACQ_MD and I_TIG of the FPRB0 must be 0**.** In this way we park the FPRB0 in the START state (see Appendix A), and so it is not going to start the readout sequence.
- Follow the diagram in Figure 4. Observe that the CK_AN clock has to have a rising and falling edge while SHIFT_IN remains stable. Details about timing of this operation are provided in "Configuration and Readout Digest", on Appendix B.
- After these steps the chip is ready for the readout, performed by the outer board.

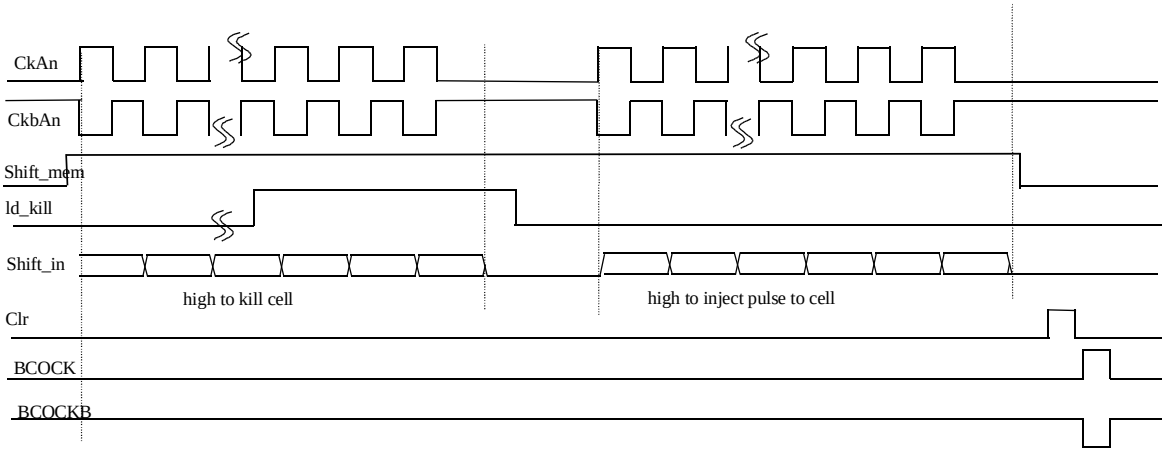

Figure 4. Initialization Sequence

2.2 Readout

2.2.1 FPRB0

When the FPRB0 receives a Trigger Input (TR_IN_SINT or TR_IN_VME) it will start the readout cycle. It may happen that no data to read out is available, in which case the FPRB0 will only transmit the start header and the end of readout identifier. More details about how the readout sequence was implemented in the EPLD can be obtained on Appendix A.

The data readout from the FPRB0 is transmitted to the STAR through an eight bit plus STAR Clock (STAR_CK) parallel cable. The VME crate controller will set the STAR to accept triggers from the scintilator (or some other source) before the data may actually become available. For this, we will use the Start Spill signal supplied by the accelerator. This signal can be interface to the CPU by means of the VME Digital I/O interface.

It is also possible to inject charge in the input of the pre-amplifiers of the FPIX0 (CHR_INJ). This is a procedure that can be used to test the sanity of the FPRB0. For this, the VME crate controller will again use the VME Digital I/O interface. Digital Outputs of this interface will set the proper masks to select different pre-amplifiers inside the FPIX0, and then trigger the charge injection. Following the charge injection, the FPRB0 automatically executes a data readout cycle.

The readout cycle comprehends four steps:

a) detection of pixel hits in FPIX0,
b) readout of Pixel address and scintilator coincidence counter (external to FPIX0),
c) followed by the analog to digital conversion of the integrated charge
d) transmission of this information to the STAR.

The VME crate controller will poll this signal through the VME Digital I/O interface, and when it is set, it will automatically inform the STAR that it has to accept triggers from the sintilators.

2.2.2 FPIX0

The FPIX0 will start the read out mode by setting ti_g. This input enables the access of pixel cells onto the internal data bus. It must be active at the beginning of the FPIX0 readout cycle. The FPIX0 responds to cell hits by asserting (low level) the chip_or signal. This event must be used by the periphery logic to initiate a readout cycle. Since there is a bug in token passing logic of FPIX0, and the chip must be reset after the end of every event, the internal FPIX0 Time Stamp register will not work as such. However,

no Time Stamping will be implemented for the FPIX0 Beam Test because the beam will not have a defined structure to be able to identify BCOs. The clr signal, which resets the FPIX0, disconnects the output data bus. As shown in Figure 5, a BCOck pulse must be provided after clr to recover the control of the output data bus.
A Scintilator Coincidence Counter will be implemented into the EPLD to keep a count of scintilator hits even when a trigger is not issued. Once an event has been "captured" by the FPIX0, all further events are disabled until the current event has been read out.

Figure 5 shows a typical read out timing sequence. The first valid data is generated in response to ti_g. The following hit outputs are triggered by to_adv signal. The time it takes the data to be valid onto the outputs is wide ranging variable. The reason is due to the fact that every time a to_adv signal is issued the token passing process is started. The worst case takes place when the current token is in the first column and the next hit cell is at the end of the last column. The output data will be synchronously readout allowing a setup time according to the worst case time.

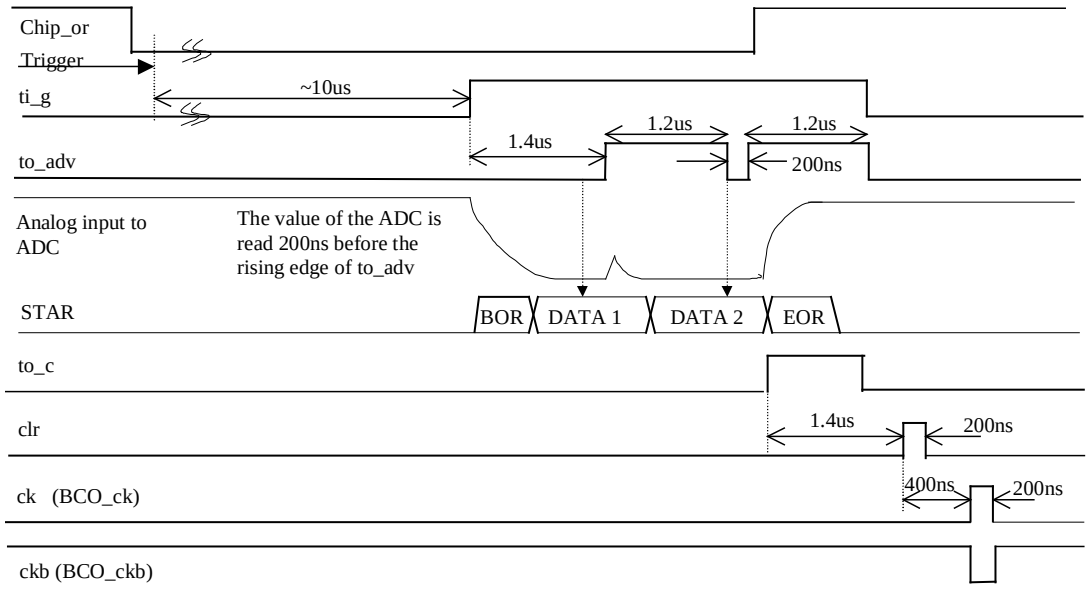

Figure 5. FPIX0 Readout Timing

3 FPRB0 INTERFACES

3.1 The RS485 Interface Port

The RS485 interface provides commands and clock to the FPRB0. Those signals are generated by the Workstation through the VME Digital I/O board (the pins assignments are shown on Table 4). The main functions through the RS485 interface are:

- **VMERESET**: FPRB0 logic reset. The Reset operation resets the FPRB0 logic to an IDLE condition and the external Time Stamp register to zero.
- **ACQ_MD**: When logic level 1 enables the FPRB0 to wait for a trigger.
- **SHIFT_MEM_I**: Load inject pattern signal.
- **LD_KILL**: Load kill pattern signal.
- **SHIFT_IN**: Programming shift register input.
- **I_TIG** : A high level in this input enables the access of pixel cells onto the internal data bus. It must be active at the beginning of the chip readout cycle.

- **CHR_INJ**: A logic level 1 injects charge in the FPIX0.
- **CLR**: This is the reset of the FPIX0, necessary after the initialization and readout sequence.
- **TR_IN_VME or TR_IN_SINT and TR_SINT_EN**: Starts FPIX0 and FPRB0 logic for readout. The FPRB0 has two trigger inputs, one generated by the coincidence of sintilators (TR_IN_SINT) and another by the VME Digital I/O board (TR_IN_VME). Internally, the EPLD in the FPRB0 Outer Board does the following logical operation with these signals: it "ands" TR_IN_SINT and TR_SINT_EN, and the output of this end is "ored" with TR_IN_VME. Therefore, in both cases, the action taken by the FPRB0 in case of a trigger is the same: it reads out the Pixel Detector and transmits the data to the STAR. The TR_IN_SINT trigger input can be disabled by the Trigger Sintilator Enable input (TR_SINT_EN) through the "and" logic. This is a useful feature if one wants to inject charge or exercise the TR_IN_VME input when there are triggers on the TR_IN_SINT. A logical level ZERO in TR_SINT_EN disables the sintilator trigger input.
- **CK_AN and BCOCK**: The Initialization logic clock (CK_AN) shifts data into the FPIX0 kill/injection shift registers. The signal coming from the RS485 interfaces is passed through the EPLD to generate a two phase clock (CK_AN,CKB_AN). The BCOCK increments the BCO counter for event time stamping. This signal is also passed through the logic to generate a two phase clock (BCOCK, BCOCKB).
- **VME_CK**: It can provide the clock to the FPRB0.

3.2 Analog to Digital Converter

The analog to digital on the FPRB0 is the Analog Device's AD775. This is a 20MSPS eight bit ADC. The most significant seven bits of the converter (Data bits 1 to 7, where 7 is the most significant bit) will be used, in order to comply with the data readout format shown in Table 2, that requires the most significant bit of the pulse height to be always logical level ZERO.

3.3 The STAR Interface

The STAR output port is an eight bit parallel port plus clock. The STAR saves the data into its own internal buffer when it detects any transition on the Readout Clock line (RD_CK). The FPRB0 incorporates a delay line to allow the adjustment of the phase of the RD_CK in relation to the data (see Figure 6). The delay line has maximum delay of 200ns in 5 taps, with 40ns of increment in each tap.

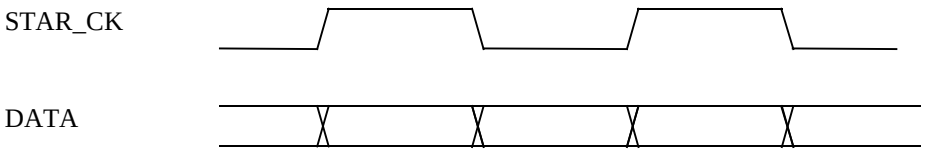

Figure 6. DATA and RD_CK relationship

3.4 Pixel Detector Data Readout Format

The data readout from the FPRB0 to the STAR will be a sequence of one byte in parallel with a clock. The bytes are saved by any transition on the clock line, i.e., low-to-high as well as high-to-low transitions. To differentiate the type of byte in the data stream, two mechanisms are used:

a) the rising or falling transition of the clock that save them into the STAR, and
b) the most significant bits that serve as identification bits.

The identification bits, as shown in Table 1, are similar to the ones used by the STAR. The objective is to avoid changes on the STAR to accommodate the data readout from the FPRB0. End of Readout (EOR) and Begin of Readout (BOR) are the two control words for the STAR defining the frame

boundary. Both of them have their MSB=1. The other words are considered data and have their MSB=0. However, an 8 bit data word could be allocated in the high-to-low transition of the STAR's clock because these words are not checked by the STAR's control logic. The 7 bit Spill Counter will provide some event separation based on spills. The Detector Coincidence Counter (DCC) accounts for Scintilator or other type of detector coincidence, even when they do not generate a trigger. An extra DCC word, a dummy word (0xxx xxx) and three extra End of Readout words (EOR) are included in the data stream to meet a 32 bit data alignment and to synchronize the low-to-high transition of the clock with the EOR.

Table 1. Control Byte and Bit Assignment

Control Byte	**Bit Assignment**
BOR	10xxxxxx[1]
Spill Counter	0ddddddd
Column Address	0000dddd
Row Address	00dddddd
Detector Coincidence Count.	0ddddddd
Pulse Height	0ddddddd
EOR	11xxxxxx

Table 2 shows a typical sequence of bytes of the data readout from the PRB to the STAR. The BOR signal indicates the beginning of the event. Then, there is a sequence of Pixel Address and Pulse Height (PH) for every hit pixel read out from the Pixel Detector. When the EPLD logic finishes the readout of all pixels, it sends the EORs.

Table 2. Readout Data Format

BOR
Spill. Count.
Det. Coinc. Count.
Det. Coinc. Count.
Column Address
Row Address
Time Stamp
Pulse Height
Column Address
Row Address
Time Stamp
Pulse Height
:
Column Address
Row Address
Time Stamp
Pulse Height
EOR
EOR
EOR
EOR

[1] "d" is data bit, "x" is don't care.

The Pixel Address is formed by two words. The Column Address is the lower four bits, and the Row Address is lower six bits. The SGI computer can append headers to the data before storing it into disk, like run setup, spill number, etc.

4 ELECTRICAL AND MECHANICAL SPECIFICATIONS

4.1 The FPIX0 chip

The FPIX0 nominal Power Supply is 3.0 volts. However, it can be operated up to 3.3 volts increasing the power consumption. Since some of the devices used in the PRB require 5 volts, the 3 volts will be generated on board with a voltage regulator.

4.1.1 Threshold Levels

The Pixel's cell threshold level is set externally to the FPRB0. The external voltage supply must have less than 10mV of precision (although 1mV is preferred), and must be very stable not to modify the threshold voltage during the run.

4.1.2 FPIX0 biasing

There are 8 biasing signals for FPIX0 but only 3 are essential: Vth, Vbbp and Vfb. They will be externally supplied by precision current sources through LIMO connectors. The other 5 are used as fine tune adjustments and will be available through a header connector at the front of the FPRB.

4.2 Input/Output

We will now describe the electrical and mechanical characteristics of the digital inputs and outputs of the FPRB0.

4.2.1 Pixel Data Readout Port Interface

The following is a description of the Pixel Data Readout Port connector signals. All the signals on this connector are implemented in PECL levels. They are "signal" and "signal*" and for the description below only the "signal" name is provided. A logical level ONE has the "signal" at its most positive level and "signal*" at its most negative level.

- DATA[0:7]: Contains the Pixel data
- STAR_CK: Readout clock is driven into this line.

Each of these interfaces implement eight unidirectional PECL differential data signals and one readout clock (with maximum speed of 26.5 MHz). The connector pin assignment is provided in Table 3. The PECL drivers are the AT&T data drivers ATT41MG, and the termination scheme should be as shown in Figure 7. The connector is a 20 pin PCB header, 100 mils flat ribbon cable connectors, right angle.

Table 3. FPRB0 Data Readout Port Pin Assignment

Pin Number	Signal	Pin Number	Signal
1	DATA[0]	2	DATA*[0]
3	DATA[1]	4	DATA*[1]
5	DATA[2]	6	DATA*[2]
7	DATA[3]	8	DATA*[3]
9	DATA[4]	10	DATA*[4]
11	DATA[5]	12	DATA*[5]
13	DATA[6]	14	DATA*[6]
15	DATA[7]	16	DATA*[7]
17	STAR_CK	18	STAR_CK*
19	GND	20	GND

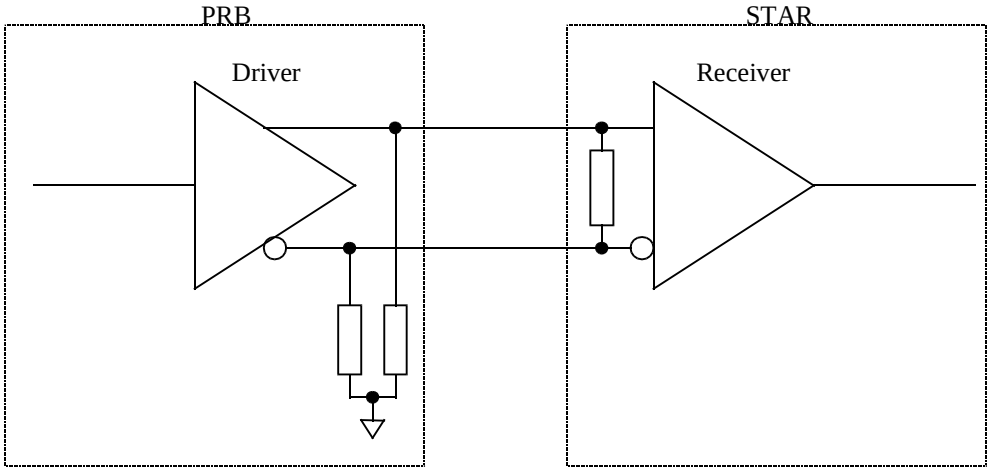

Figure 7. Data Input Termination Used for the STAR

4.2.2 Sintilator Trigger and Clock Inputs

As said in section 3, the FPRB0 has two trigger inputs. The Scintilator trigger (TR_IN_SINT) and the Scintilator trigger enable (TR_IN_SINT_EN) signals are combined with the VME trigger inside the FPRB0. Two different electrical protocols will be available to interface the TR_IN_SINT and CLK signals: ECL and NIM. The following subsections define the ECL and NIM connections at the receiver end, on the FPRB0 outer board.

4.2.2.1 ECL Sintilator Trigger and Clock Inputs

These inputs are differential ECL designed for a 120 Ω flat ribbon cable, as shown in Figure 8. Observe that the ECL outputs of the drivers need to be biased on the driver side. One such standard model that has this feature is the NIM Model 4616, 16 Channel ECL/NIM/ECL Converter from LeCroy. The connector is a 10 pin PCB header, 100 mils flat ribbon cable connectors, right angle.

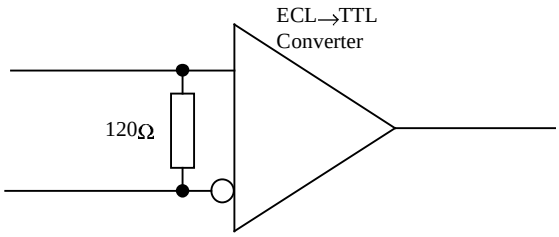

Figure 8. ECL Inputs

4.2.2.2 NIM Sintilator Trigger and Clock Inputs

These inputs are in current mode converted to TTL levels by a 50 Ω resistor and a MAX 901 comparator as indicated in the Figure 9. Four NIM inputs will be available through LIMO connectors: TR_IN_NIM, CLK_NIM and two spares (SP1_NIM, SP2_NIM).

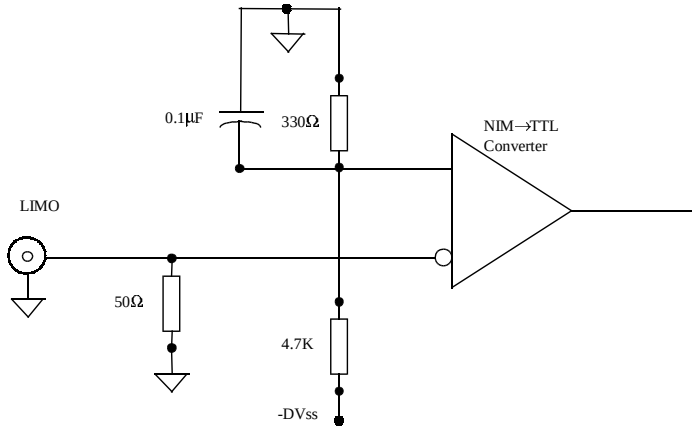

Figure 9. NIM Input

4.2.3 RS485 Inputs

The FPRB0 receives command and control signals from the RS485 VME Digital I/O board (see Reference [7]). This VME Digital I/O board has a 50 pin PCB header, 100 mils flat ribbon cable connectors, right angle, with all RS485 digital I/O's, additional controls and external clock. The connector on the FPRB0 side will be a 26-pin header, 100 mils flat ribbon cable, right angle, with no ears to remove the header. Table 4 shows the pin assignment for this connector.

Table 4. RS485 Input Pin Assignment

Pin Number	Signal	Pin Number	Signal
1	VMERESET	2	VMERESET*
3	ACQ_MD	4	ACQ_MD*
5	SHIFT_MEM_I	6	SHIFT_MEM_I*
7	LD_KILL	8	LD_KILL*
9	SHIFT_IN	10	SHIFT_IN*
11	CK_AN	12	CK_AN*
13	TR_IN_VME	14	TR_IN_VME *
15	TR_SINT_EN	16	TR_SINT_EN*
17	BCOCK	18	BCOCK*
19	I_TIG	20	I_TIG*
21	CLR	22	CLR*
23	CHR_INJ	24	CHR_INJ*
25	VME_CK	26	VME_CK*

4.3 Mechanical FPRB0 printed circuit board requirements

The FPRB0 will be designed in two pieces, the Inner Board" and the Outer Board. The Inner Board will hold the FPIX0 chip the ADC and the 3 volt power supplies. All the other components will be located in the outer board. The purpose of the Inner Board is to be able to change a non working FPIX0 chip without having to worry about loosing the motherboard until this change is done or having to have many working FPRBs with different FPIX0 chips. The interface between the Inner and Outer Board is a 50 pin ribbon cable.

The Inner Board dimensions are 5'' by 8'', and the Outer Board dimensions are 5.5" by 5.5".

A coordinate convention has been established as follows: X axis is drawn along the longest side of the board (8"), Y axis along the shortest side (5") and Z normal to the X-Y plane (see Figure 10).

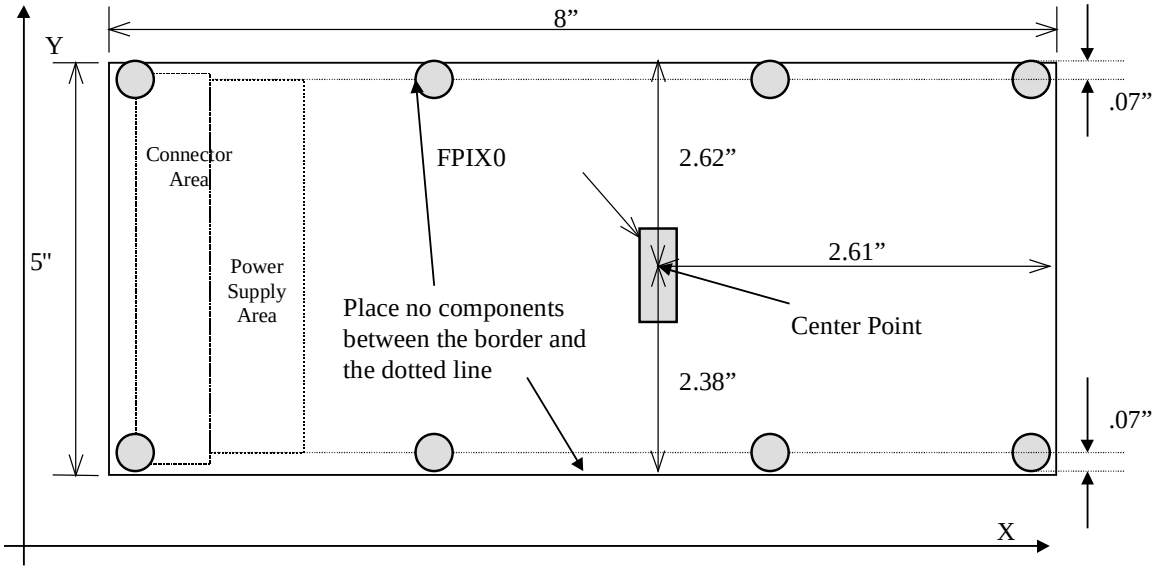

Figure 10. FPRB0 Dimensions

The FPRB0 Inner Board will be placed in grooves into a specially designed 7.5" by 5.62" by 15.75" metal-box (x-y-z coordinates, respectively). As a consequence, 2.38" of the FPRB0, by the connector area, will exceed the box dimensions. The FPIX0 will be placed with its longer side along the X axis, as shown in

Figure 12. The exact placement is defined by a *center point* at 2.610" from the left side and 2.387" from the bottom side. This center point corresponds to the center of an *active area* defined on the chip, where the *detector* is located. The FPIX0 size is 0.210" by 0.248" (5.342mm by 6.320mm) and the Pixels *detector* active area size is 0.126" by 0.190" (3.21mm by 4.82mm). The bump-bonded detector is about 3 times the size of the Pixel amplifier chip. The detector covers 10 of the 12 *active area* columns.

The PC board thickness will be thinned in order to reduce the amount of maze underneath the *active area*. A hole is not practical for two reasons: the back of the chip (substrate) must be grounded, and the active area is very close to two of the edges of the FPIX0 chip. An absolute error of 10 mils will be allowed on each side of the *detector* in order to align it with the *active area*.

FPIX0 orientation: The bump-bonded pixel detector is about 3 times bigger than the FPIX0 chip. The pixel detector and chip are arranged as shown in Figure 11.

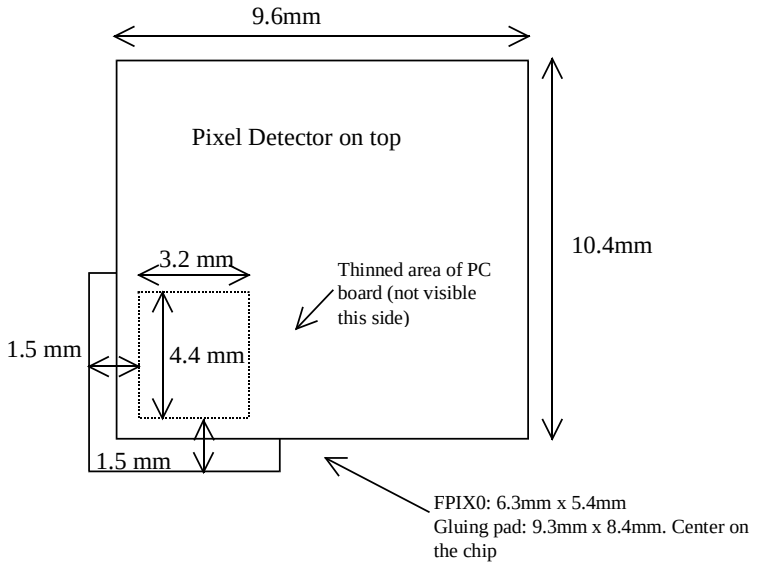

Figure 11. Pixel detector and amplifier chip setup

Figure 12 shows the orientation of the Pixel chip respect to the PC-board. The only side without pads must face the bottom side of the board as shown. This figure also shows the absolute coordinates of the active area, Pixels chip, and plastic protecting case, respect to the bottom-right corner of the board. A plastic case will protect the Pixel chip against all kind of manipulations around it. No components, but some bypass capacitors, will be located in that area.

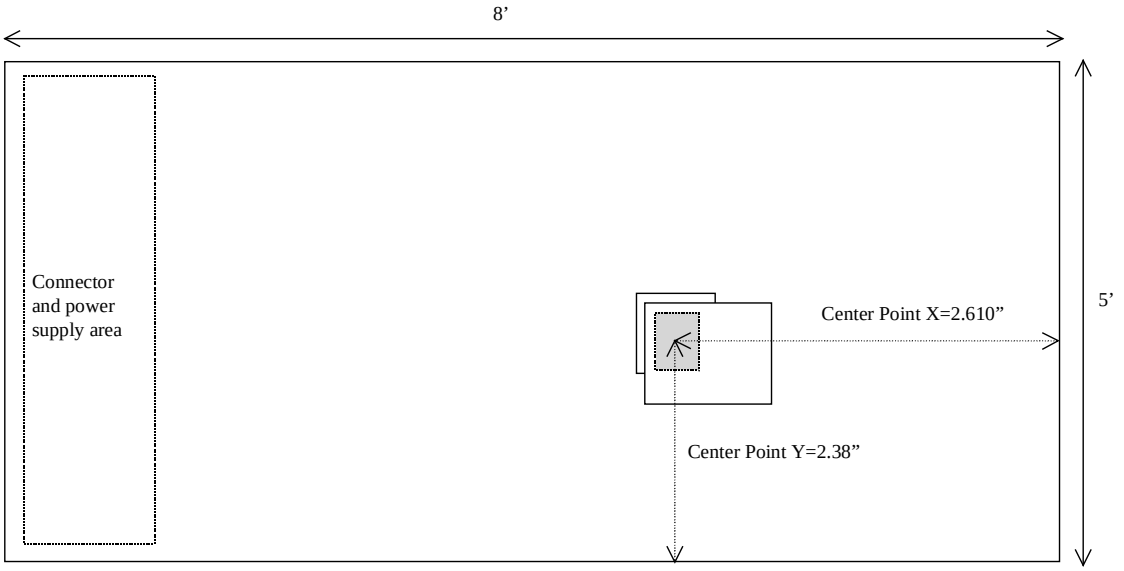

Figure 12. Pixel Chip Orientation

The box will have various grooves to allow the PRB to rotate on its Y axis making 15, 30 and 45 degree angles respect to the X-Y plane. Care must be exercised to align the pixels chip in all different situations.

Figure 13 shows a transversal cut of the Pixel detector, chip and PC board assembly

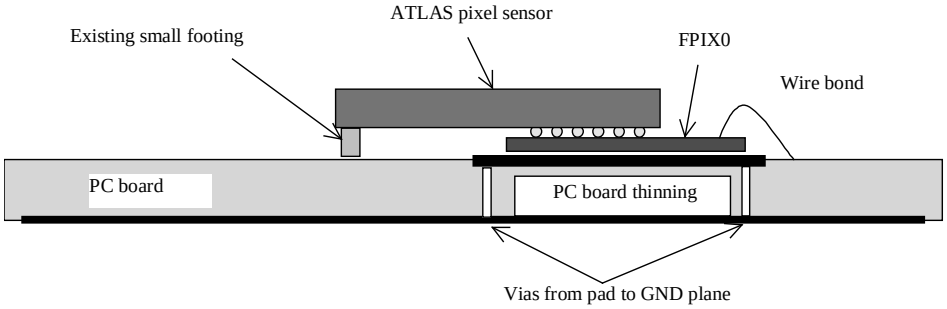

Figure 13. Pixel detector, Chip and PC Board Assembly

Due to wire-bonding requirements, only low profile components will be allowed to be closer than 1.95” from the center of the Pixels chip. The maximum height for a chip in the low profile area is defined to 0.225” (5.7mm). Also, 125 mil holes are needed on each corner for holding the board at assembling time.

The FPRB0 can assemble components on top and bottom. This is particularly interesting to mount small surface mount capacitors and resistors. Specifically, the .1uF decoupling capacitors must be as close as possible to the chip.

Other important PC board layout considerations are:

- There must be analog and digital ground points accessible at certain locations in order to make a common (unified) ground. These points must be: at the ADC, at the power regulators, at the Pixels chip.

- The solder mask around the end of the wire bondable 3 mil traces must allow a minimum opening of 12 mils to work as wire bonding pads. However, the very end of those traces must be protected with the solder mask, as shown in Figure 14, to avoid 3-face etching problem.

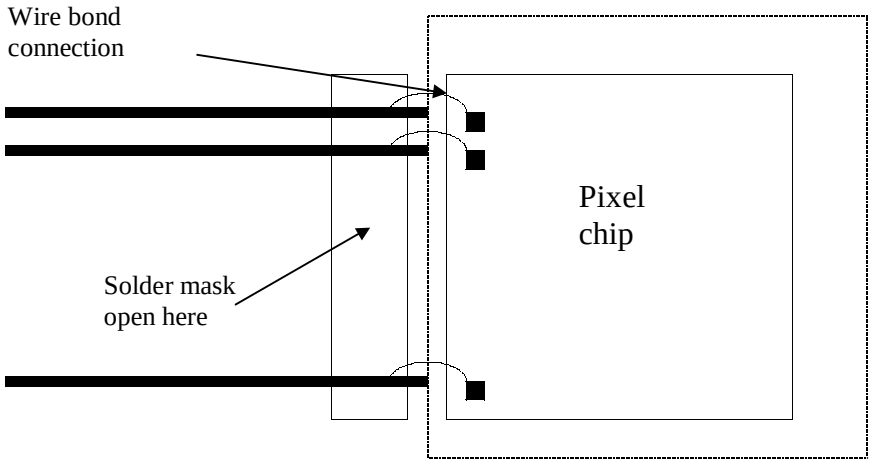

Figure 14. Solder Mask Details

- There will be a ground and power plane open area at the Pixels chip to allow for the *active area hole*. The power plane can be started right at the same distance from the *center point* where the 3 mil traces start.
- A wire bonding practice area, as shown in Figure 15, will be placed on the board to test the wire bonding conditions, materials, etc.

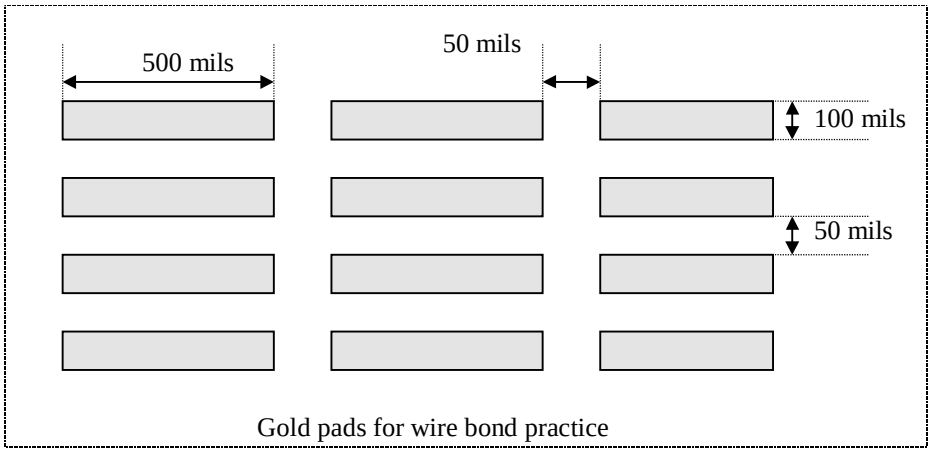

Figure 15. Wire Bond Practice Area

4.4 Power Supplies Requirements

The FPRB0 requires power supplies as shown in Table 5. The ground of the +5.0 V digital section and the ground of the –5.2 V should be connected together. The ground for the analog sections should be a separate ground, connected just to one point to the digital ground. The internal 3.0 V for the analog and digital sections is obtained by a voltage regulator with low voltage drop, the Micrel MIC2941A.

Table 5. Power Supplies

Voltage	Current (max.)	Usage
+5.0 V	100mA	Analog sections
+5.0 V	1.8A	Digital sections
–7V	10mA	Analog buffer
–5.2 V	300mA	ECL to TTL converters

4.4.1 Module Fusing & Transient Suppression

All three power supplies have to be properly fused. In addition, Transorbs should be included to protect against over-voltage conditions on each power supply.

5 APPENDIX A: EPLD Firmware

5.1 Introduction

This appendix describes the firmware implementation for the readout logic of the Pixel Readout Controller Board (FPRB0) with the 1st Fermilab Pixel chip. In Figure 16 see the different parts of the project: seven latches, one counter, one AND, one OR and two NOTs belong to the Hardware. This specific Hardware, written in VHDL, treats the inputs and outputs to the Logic Unit. In the Logic Unit these signals are used to complete all the steps to the FPIX0 read out.

5.2 Hardware

- Trigger (TR_SINT_EN, LT_TR_IN_SINT, LT_TR_IN_VME): The TR_SINT_EN comes directly from the RS485, while LT_TR_IN_SINT and LT_TR_IN_VME are latched. The logic used to deal with these signals is very simple. The Trigger that the EPLD recognizes is the combination of these three signals in a way that both LT_TR_IN_SINT (that comes from the scintilators) or LT_TR_IN_VME (from the VME interface) can start the read out. But if the TR_SINT_EN is zero than LT_TR_IN_SINT should not be considered.

- BCO Counter (I_BCOCK): This counter is used to send to STAR the number of scintilator coincidences after the start of spill. After a trigger signal this value is latched, and then the Logic Unit reads it to build the header frame.

- Signal Logic (I_CKAN , I_BCOCK , BCOCK_5V , BCOCKB_5V , CKAN_5V, CKANB_5V): The signals I_CKAN and A_BCOCK are passed through the EPLD to generate the two face outputs BCOCK_5V, BCOCKB_5V, CKAN_5V and CKANB_5V.

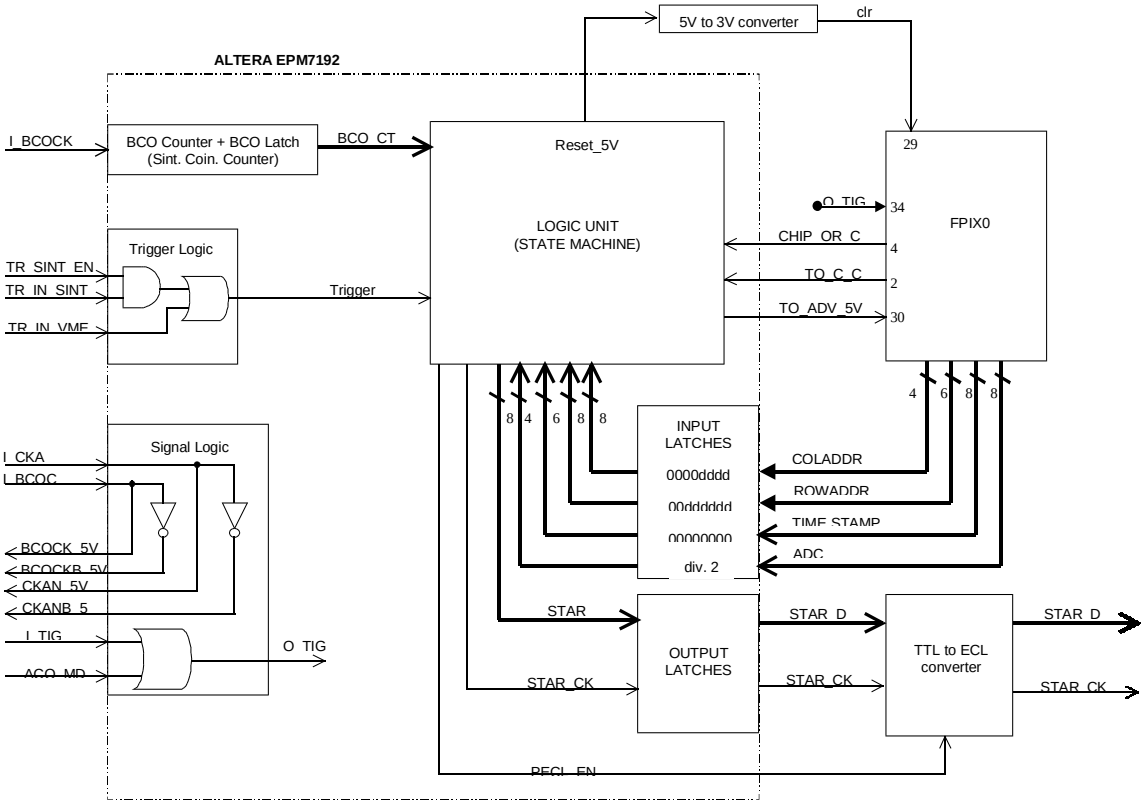

Figure 16. Block Diagram of Part of the FPRB0 Controller

5.3 Logic Implementation

The logic necessary to complete the FPIX0 read out in the PRB0 will be implemented as a Moore state machine, where the outputs may change only with a change of state. The Figure 17, Figure 18 and Figure 19 show the detailed flowchart to make this machine:

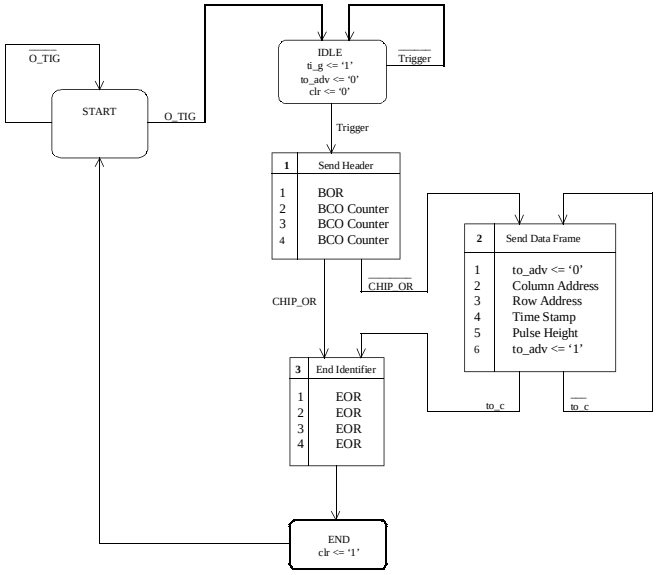

Figure 17. State Transition Diagram

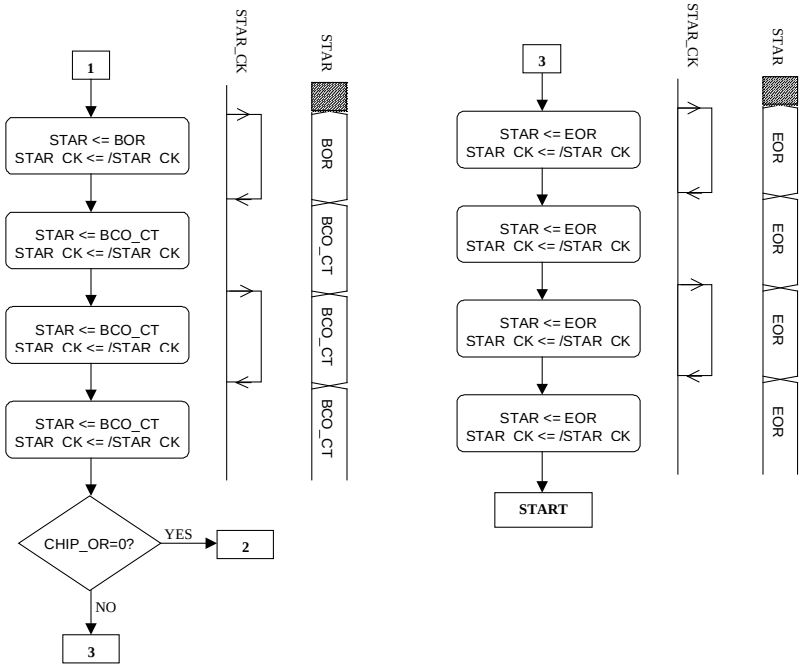

Figure 18. States 1 and 3

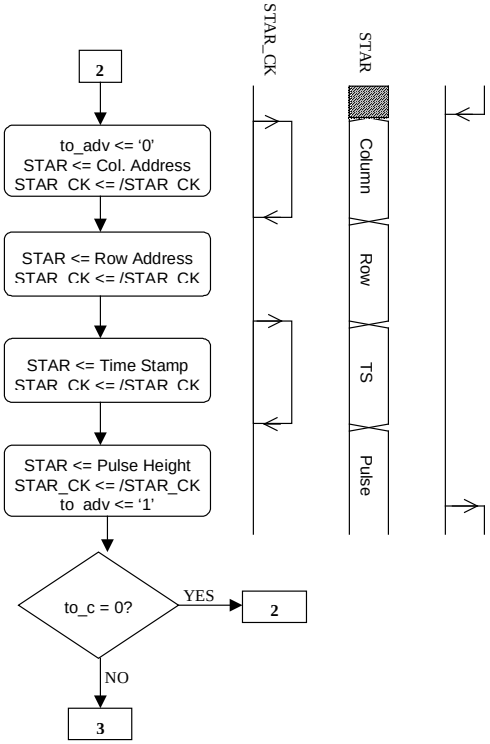

Figure 19. State 2

6 APPENDIX B: Configuration and Readout Digest

The following document describes the software that will communicate with the outer board. The first step that must be done by the STAR is the initialization of the FPIX0. After that it has to wait for a read out sequence from the outer board.

6.1 INITIALIZATION

The initialization of the FPIX0 has to be done in two phases. The first phase will load the chip with the kill pattern, and the second one will inject a pulse in the cells. So, something like this must be written in the software:

Start of initialization

ACQ_MD = 0;
I_TIG = 0;
Shif_mem = 1;

Generate 768 cycles of clock in CkAn, and for each of these cycles shift_in must be high if you want to kill the cell, or low with you don't.

For (i =0,i =767)
Pulse CkAn , Shift_in

If i=760 then ld_kill = 1
End

Wait > 500ns

ld_kill = 0

Wait > 500ns

Repeat the same loop, but now shift_in will be used to enable the charge injection to the cell

For (i =0,i =767)
Pulse CkAn , Shift_in

End

Shift_mem = 0

End of initialization.

6.2 READOUT

To start the readout cycle, ACQ_MD or I_TIG must be 1, and the combined trigger input (see Appendix A) also must be 1. The clock and data to STAR are sent for the outer board. So the STAR must wait for every edge of this signal (STAR_Ck) to read a valid data. After the first edge, Table 6 shows the frame that will be send by the outer board:

Table 6. Beginning of Readout

1st byte	BOR (10XXXXXX)
2nd byte	Spill counter
3rd byte	BCO counter
4th byte	BCO counter

Then the outer board can send a frame of data or the end identifier. If there is a hit, the data frame will be send the sequence shown in Table 7.

Table 7. Data

1st byte	Column Address
2nd byte	Row Address
3rd byte	Time Stamp
4th byte	Pulse height

Otherwise, if there are no hits, or the FPRB0 has no more hits to send to the STAR, the end identifier is send (as shown in Table 8).

Table 8. End Identifier

1st byte	EOR
2nd byte	EOR
3rd byte	EOR
4th byte	EOR

7 APPENDIX C: FPIX0, THEORY OF OPERATION AND OPERATION MODES

Figure 20 shows a photograph of the FPIX0 chip. Next sections will describe the features this chip.

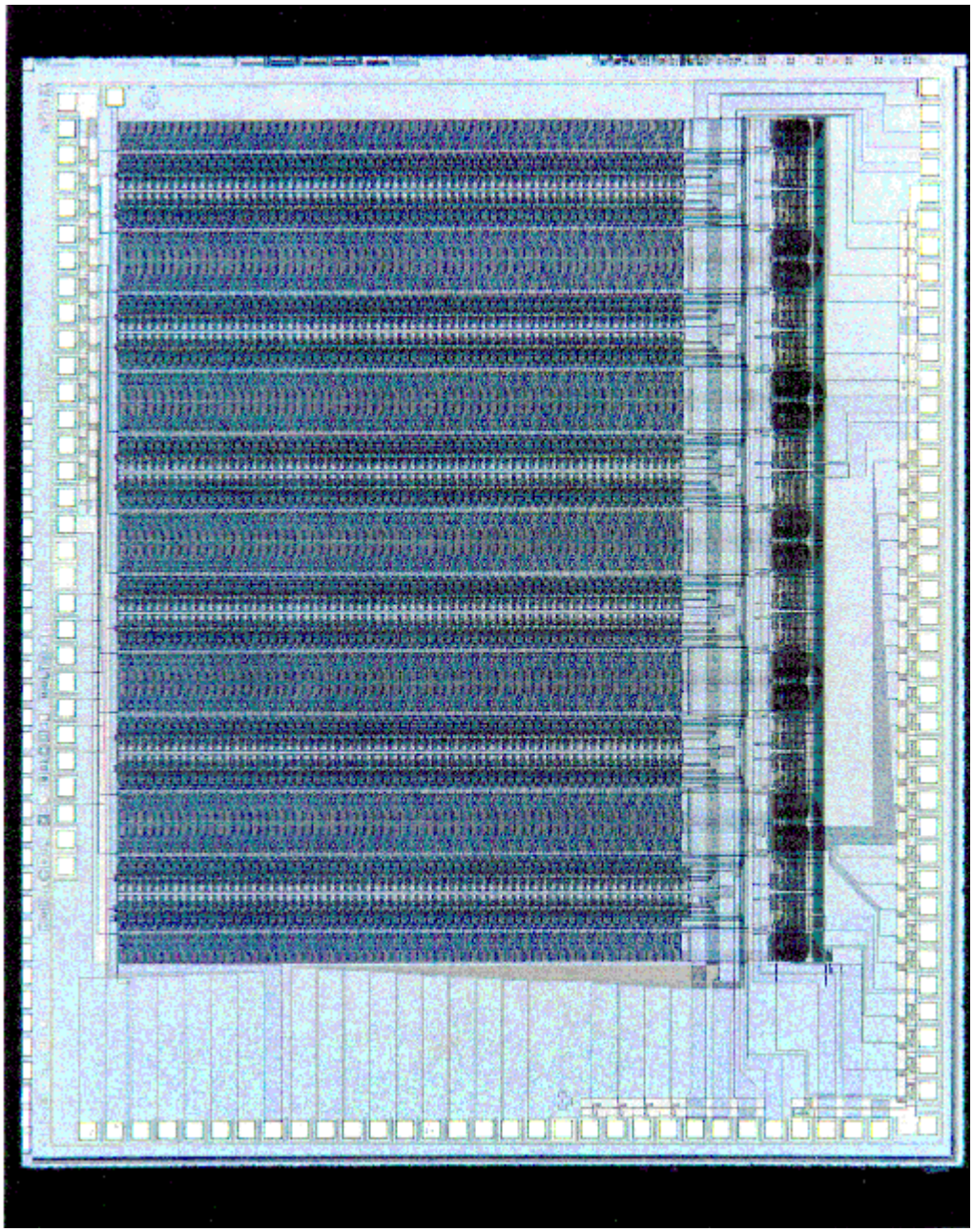

Figure 20. FPIX0 Photo

7.1 SHORT DESCRIPTION OF FPIX0

FPIX0 is a Front-end Amplifier/Discriminator Array for Pixel-based detectors. FPIX0 is the first prototype of its kind designed at Fermilab. The fundamental objective is to gain experience toward the design of a complete Preamplifier, Discriminator and Controller chip for Pixel-based Detector Systems.

The FPIX0 pixel matrix array has 12columns with 64 pixels each. The cell size is 50μ by 400μ, compatible with the pixel size of the detectors used in ATLAS. These detectors have been successfully bump-bonded to FPIX0. Both the *bare-chip* and the *bump-bonded* versions of FPIX0 have been characterized during 1997-1998 [9], [10]. The following objective is to test FPIX0 in the beam at Fermilab during 1999.

The front-end amplifier is located in the pixel cell and has two *folded-cascode* stages. The two stages are AC coupled and the output of the second stage is DC coupled to the discriminator. The first stage is a charge amplifier that uses a current controlled active feedback circuit (Marseille type). The feedback current controls the return-to-baseline time and leakage compensation. The second stage provides additional gain and buffers the preamplifier. The threshold is independent of the leakage induced DC shift in the preamplifier. The discriminator is a classic two stage comparator.

The cell logic stores the hit in a SR Flip-Flop, asserts the Fast_OR and waits for an external token signal. Upon token reception, it generates:

Getbus signal that enables the address switches to take the global bus.

Sample/Getbus signal for the peak circuit to take the Global Analog_out line.

Upon Token_adv signal, the logic clears itself and the peak circuit automatically. The token is passed to the next hit pixel (if any). The EOC logic stores the content of the BCO counter in the BCO register and disables the column until read out.

The digital and analog outputs of the top row of FPIX0 are externally provided for diagnostic purpose. The Pixel array contains two different kind of cells, one with *nominal* values and another with lower feedback capacitance (VLCf) to provide higher gain and lower noise but with, probably, higher cross-talk.

7.2 FPIX0 General Characteristic Values

- Power Supply (*nominal*): 3 volts.
- Power consumption: 36μwatts/cell.
- Front-end rise time: 40 ns (10%-90%).
- Front-end recovery time: 545 ns (10%-90%).
- Noise: 50 e- rms (36 e- for VLCf).
- Minimum Threshold: 700 e- (500 e- for VLCf).
- Maximum Threshold: “infinite” in voltage mode.
- Threshold spread nominal: 227 e- rms (100 e- optimized).
- Threshold spread VLCf: 145 e- rms (<100 e- optimized).
- 2 bias currents, 1 voltage threshold controls.
- Noise of FPIX0 with bump-bonded detector: 95 e- rms (77 e- for VLCf).
- Threshold spread nominal with bump-bonded detector: 500 e- rms.
- Threshold spread VLCf with bump-bonded detector: 165 e- rms.

7.3 Description of FPIX0 signals

Token based signals

2	to_c	Digital out	Token out signal (diag)
30	to_adv	Digital in	Token advance signal (handshake)
34	ti_g	Digital in	global token in (handshake)

ti_g: A high level in this input enables the access of pixel cells onto the internal data bus. It must be active at the beginning of the chip readout cycle.
NOTE: **ti_g** can be used as a "beginning of acquisition mode" input in the FPRB0. It can also be permanently connected to Vdd to keep the token always enabled.
to_c: indicates that no more hits are to be readout and the token is passed to the next chip. This signal can be used to indicate the end of readout. However, it has never been tested before. Other "artificial" end-of-readouts can be programmed in software by checking the pixel address until the same address is readout or by reading a fixed number of pixels.
to_adv: this signal must be used as the readout clock. It starts the token passing from cell to cell. It automatically skips the cells without hits. It can go as fast as 5 MHz but if we are using analog output, it must go slower (1 MHz maximum).

Hit Indicator. Wired OR of all pixels

4	chip_or	Digital out	Chip hit indicator (handshake)

This signal is a wired-OR of all pixel comparators in the chip. It indicates hit presence.
NOTE: There is a problem with this signal. It does not go up (inactive) after the last pixel has been readout and must be reset by the **clr** signal.

Valid data indicator

5	val	Digital out	Valid data indicator (handshake)

It indicates that the digital data outputs (i.e. **ColAddr**, **RowAddr**, and **Tstamp**) are valid on the bus.
This signal is too slow to be used as a handshake signal for pixel readout. The pixel readout must be synchronous and adjustable in clock speed. The rising edge of the readout clock (**to_adv**) will enable the pixel's digital and analog outputs. The falling edge can be used to latch and/or convert the data.

Output Data Signals

7	gb[3]	Digital out	ColAddr[3] (data out)
8	gb[2]	Digital out	ColAddr[2] (data out)
9	gb[1]	Digital out	ColAddr[1] (data out)
10	gb[0]	Digital out	ColAddr[0] (data out)
11	gb[11]	Digital out	RowAddr[7](data out) (NC)
12	gb[10]	Digital out	RowAddr[6](data out) (NC)
13	gb[9]	Digital out	RowAddr[5](data out)
14	gb[8]	Digital out	RowAddr[4](data out)
15	gb[7]	Digital out	RowAddr[3](data out)
16	gb[6]	Digital out	RowAddr[2](data out)
17	gb[5]	Digital out	RowAddr[1](data out)
18	gb[4]	Digital out	RowAddr[0](data out)
19	gb[12]	Digital out	Tstamp[7](data out)

20	gb[13]	Digital out	Tstamp[6](data out)
21	gb[14]	Digital out	Tstamp[5](data out)
22	gb[15]	Digital out	Tstamp[4](data out)
23	gb[16]	Digital out	Tstamp[3](data out)
24	gb[17]	Digital out	Tstamp[2](data out)
25	gb[18]	Digital out	Tstamp[1](data out)
26	gb[19]	Digital out	Tstamp[0](data out)

These signals provide Pixel Column, Pixel Row and Time Stamp information. These outputs change with the rising edge of **to_adv** clock.
NOTE: The timing from the rising edge of **to_adv** to valid data **is variable** because the token passing process is involved in this cycle. The enabling of the digital information itself is fast (~20ns) but this cycle may take long if after reading one of the first pixels of the first column, the next pixel is one of the last pixels of the last column. The worst case readout time can be as long as 200 ns.

The Time Stamp information is stored in a register at the periphery. Newer Time Stamped hits are disabled until the current Time Stamped hits are readout.

Reset signals

29	clr	Digital in	Reset

The **clr** signal is active high. It resets the content of all pixel cell Flip-Flops and BCO counter (i.e Time Stamp information). The Kill/Injection Logic **is not** reset by the **clr** signal

Clock signals

32	ck	Digital in	BCO clock
33	ckb	Digital in	BCO clock bar
91	ckAn	Digital in	Programming clock
92	ckbAn	Digital in	Programming clock bar

The rising edge of BCO clk advances the TS counter.

ckan is the clock of the programming shift register. This SR permits to select a particular pixel for injection (that pixel will see the input signal) and/or for the kill operation. The kill operation will suppress the digital output of the programmed pixel whether it has a signal or not. The injection pattern can be programmed at any time without altering the kill pattern. However, if the kill pattern is to be reprogrammed, the injection pattern NEEDS to be reprogrammed too. The nominal frequency recommended for **ckan** is 1MHz. Although, the SR works at a much higher frequency (50MHz).

ckban is the complementary logic value of **ckan**.

Chip Initialization signals

35	shift_in	Digital in	Programming shift register input.
93	ld_kill	Digital in	Load kill pattern signal
94	shift_mem	Digital in	Load inject pattern signal
99	shift_outL	Digital out	Programming shift register output

shift_in is the input of the SR. The injection/kill pattern to be programmed is to be presented at this input. The matrix is to be viewed as a long shift register of length 768 (=12x64). This register runs from the bottom of the rightmost column (bit 0) to the bottom of the last column (bit 768). The register has a serpentine pattern: the top of column 0 (the rightmost) is chained with the top of column 1, runs to the bottom of column 1 and is chained with the bottom of column 2 and so on. To program cell j of the SR a "1" is to be presented at the **shift_in** input at time (768-j*T). T is the clock period.

load_kill is the input that causes the content of the SR to actually be stored in the kill flip-flop (by going low). It must go high before the end the shift operation. When high the kill FF is transparent. It must also go low before the 769th clock edge (if any).

shift_mem is the signal that causes the SR content to be stored as the injection pattern. It must be high during the shift operation, even when shifting the kill pattern. It must go low at the end of the injection shift operation (which always comes after the kill operation, if any). A typical programming scenario is the following:
=> **shift_mem**=1; **ld_kill**=1; start shifting the kill pattern; after the 768th period make **ld_kill** go low. Start a new shift operation (for the injection pattern); after the last period **shift_mem** must go low. In the steady state **shift_mem**=0 and **ld_kill**=0.

Digital Buffer Test Output signals

56	outtestDBuf	Digital out	Digital Buffer test output
57	intestDBuf	Digital in	Digital Buffer test input

These signals are for testing purpose only. **intestDBuf** must be connected to GND trough a 50Ω resistor. **outtestDBuf** must be not connection in the FPRB

Analog Input and Output

39	inject_in	Analog in	Injection input
88	analogOUT	Analog out	Peak detector system output.

Analog input: This is a **50Ω terminated signal.** It should be accessible through a LEMO connector.
Analog Output: **AnalogOUT** signal is a voltage output. 0 volt indicates no hit. The **AnalogOUT** dynamic range is from 0 to 1.5 volts. The higher its value the lower charge in the pixel cell. **AnalogOUT** must be connected to a "standard connector".

Discriminator Output signals

44	outdis[0]	Digital out	Discriminator 0 output
45	outdis[1]	Digital out	Discriminator 1 output
46	outdis[2]	Digital out	Discriminator 2 output
47	outdis[3]	Digital out	Discriminator 3 output
48	outdis[4]	Digital out	Discriminator 4 output
49	outdis[5]	Digital out	Discriminator 5 output
50	outdis[6]	Digital out	Discriminator 6 output
51	outdis[7]	Digital out	Discriminator 7 output
52	outdis[8]	Digital out	Discriminator 8 output
53	outdis[9]	Digital out	Discriminator 9 output
54	outdis[10]	Digital out	Discriminator 10 output
55	outdis[11]	Digital out	Discriminator 11 output

These signals output the discriminator for every column of the top row cells in the chip. They are for testing and calibration purpose only. They must be connected to a standard connector to be able to connect an oscilloscope or a logic state analyzer.

Power supply and ground signals

1	vdddpad	Supply (+)	VDD supply for the I/O pad circuits (VDD)
28	vddd	supply(+)	Digital vdd (VDD)
42	vddd2	supply(+)	Digital supply for the test cells (VDD)
100	vddd	supply(+)	Digital vdd (VDD)
36	vdddpad	supply(+)	Digital vdd (VDD)
37	vdda2	supply(+)	Analog vdd2 (VDDA2)
38	vdda1	supply(+)	Analog vdd1 (VDDA1)
96	vdda1	supply(+)	Analog vdd (VDDA1)
97	vdda2	supply(+)	Analog vdd2 (VDDA2)

VDD: This is the only power source in the system. **There should be a solid VDD plane adjacent to at least one solid ground plane**. All digital Vdd's (or simply VDD) and vdda2's should be directly connected to the VDD plane and decoupled by a 1nF capacitor (at each node) to ground. The concerned pads are the 1, 28, 36, 37, 42, 100, 97. The VDD plane should be decoupled to ground by 3 4.7μF capacitors in parallel.

VDDA: This the analog VDD (VDDA). These nodes should be connected through a 1Ω resistor (0.1%) to the VDD plane. They should be decoupled by a 2.2 μF capacitor. The pads are: 38,96.

6	vsubdd	gnd	Substrate contact digital section (GND)
27	vssd	gnd	Digital vss (GND)
31	vssdpad	gnd	VSS of I/O circuits (GND)
40	vssa	gnd	Analog vss (GND)
41	vee	suply2	Analog supply for the test cells (VEE)
43	vssd2	gnd	GND
58	vshdiag	gnd	GND
59	vsubpad	gnd	GND
60	vsubpad	gnd	GND
70	vsubpad	gnd	GND
71	vsubpad	gnd	GND

79	vee	suply2	Analog supply for the test cells (VEE)
90	vsubpad	gnd	GND
95	vssa	gnd	GND
101	vssd	gnd	GND
102	vssdpad	gnd	GND

GND: There should be only one ground in the system (**at least one solid ground plane**).
All signals described as GND should be connected to the ground using the shortest trace possible. The concerned FPIX0 pads are the 6, 27, 31, 40, 41, 43, 58, 59, 60, 70, 71, 79, 90, 95, 101, 102. Note that pad 41 and 79 are called VEE in the table.

Analog Test Output signals

61	out2[0]	Analog out	analog output
62	out2[1]	Analog out	analog output
65	out2[2]	Analog out	analog output
66	out2[3]	Analog out	analog output
67	out2[4]	Analog out	analog output
68	out2[5]	Analog out	analog output
69	out2[6]	Analog out	analog output
72	out2[7]	Analog out	analog output
73	out2[8]	Analog out	analog output
74	out2[9]	Analog out	analog output
75	out2[10]	Analog out	analog output
76	out2[11]	Analog out	analog output

These signals output the discriminator for every column of the top row cells in the chip. They are for testing and calibration purpose only. They must be connected to a standard connector to be able to hook up an oscilloscope.

Analog outputs A : These are 14 sensitive analog outputs (out2[0]-out2[11], outcal1 and outcal2). Each such a signal is to be connected to a 1.2KΩ[2] (<= 1%) and to a "standard connector" (signal and ground). The other terminals of the resistors are connected to a common node connected to a 10Ω(<= 1%) resistor and decoupled to ground by a 4.7uF capacitor. The other terminal of the 10Ω resistor should accessible via a LEMO cable. (See schematic Analog output A). The chip pads are the 61, 62, 63, 65, 66, 67, 68, 69, 72, 73, 74, 75, 76, 77.

Analog Calibration Input and Output signals

63	outcal2	Analog out	Analog calibration OUT (2)
64	incal2	Analog in	Analog calibration IN (2)
77	outcal1	Analog out	Analog calibration OUT (1)
78	incal1	Analog in	Analog calibration IN (1)

These signal are for calibration of the front-end stage. **incal1** and **incal2** must be connected to GND trough a 50Ω resistor. **outcal1** and **outcal2** must be not connection in the FPRB

[2] Or closest value.

Guard ring and shield connections

89	guard	Analog out	LEM_GRD (guard I/O)
98	vshield	Analog in	VSH (shield signal gnd/in)

Analog outputs C : Guard signal. It is to be connected to a 100Ω(<= 1%) resistor and decoupled to ground by a 4.7uF capacitor. The other resistor terminal should accessible through a LEMO connector.

Shield connection must be connected to GND trough a 50Ω resistor.

Analog Bias and Control signals

80	vfb	Analog Bias	LEM_IF (feedback current)
81	vbbnl	Analog Bias	LEM_INL (1^{st} stage load current)
82	vbbp	Analog Bias	LEM_IP (2^{nd} stage input current)
83	vbth	Analog Bias	LEM_ITH (threshold current)
84	vbbpl	Analog Bias	LEM_IPL (2^{nd} stage load current)
85	vbbn	Analog Bias	LEM_IN (1^{st} stage input current)
86	vbbnComp	Analog Bias	LEM_INC (Comparator current)
87	vth	Analog Bias	LEM_VTH(threshold output voltage)

Analog Bias and Control: Each signal should be decoupled to ground by 1nF capacitor and should be accessible through a LEMO connector.

The fundamental signals are: **vfb**, **vbbp**, and **vth**. The other signals are optional. They will not be available in the FPRB0.
The master bias **current VBBP**: 14μA nominal. This is the current that sets all the needed currents inside the chip. These other currents can be also be altered using the optional bias currents. This is a negative current. It flows from the chip to the biasing source (The biasing source is ideally a current source).

The feedback **current VFB**: 2-10nA. Higher lower currents (0) can be used. This is also a negative current. It flows from the chip to the biasing source (The biasing source is ideally a current source).

The threshold **voltage VTH**: by adjusting this voltage the threshold of all pixels will be changed. VTH is about 2V nominally (This varies from chip to chip). The lower it is the higher is the threshold. At 0V (the lowest value) no pixel will fire.

The accuracy of Vth must be in the 10mV range (although 1mV range is preferred). A long term voltage stability is needed. Ideally, this voltage should be provided externally to the FPRB0 by an on-line (GPIB) computer controlled voltage supply.

8 REFERENCES

[1] Zimmermann, S., *et. al.*, "Test stand for the Silicon Vertex Detector of the Collider Detector Facility," IEEE Trans. Nuclear Science, Vol. 43, No. 3, pp. 1170-1174, June 1996.
[2] Yarema, R., "A beginners guide to the SVXII," Fermilab Doc., May 1994.
[3] Talk with David Anderson
[4] Gay, C., Huth, J., Oliver, J., Spiropulu, M., "Silicon Test Acquisition and Readout Module (STAR)," Harvard University Doc., 1994.
[5] Zimmermann, S., Andresen, J., Chramowicz, J., Gonzalez, H., Treptow, K., Zmuda, T., "Test Fiber Interface Board," Fermilab Doc., July 1995.
[6] Gonzalez, H., Treptow, K., Zimmermann, S., Andresen, J., "Test Port Card," Fermilab Doc., Aug. 1995.
[7] GrenSpring Computers Catalog, IP Carrier VIPC610 and IndustryPack IP-UniDig-D, Menlo Park, CA, 1996.